CLAIMS

I claim:

1. A data communication method for receiving digital data on a data terminal, comprising:

receiving data pulses indicative of the digital data to be transmitted at the data terminal, the data pulses having a first pulse separation to represent a first logical data value and a second pulse separation to represent a second logical data value;

generating a voltage ramp signal having a voltage magnitude between a first voltage and a second voltage;

resetting the voltage ramp signal to the first voltage a first delay after the leading edge of each data pulse;

regenerating the voltage ramp signal towards the second voltage a first time period after the resetting of the voltage ramp signal;

detecting the voltage value of the voltage ramp signal at the leading edge of each data pulse;

generating a data output signal associated with each data pulse having a first logical state when the voltage value of the voltage ramp signal is less than a threshold value;

generating a data output signal associated with each data pulse having a second logical state when the voltage value of the voltage ramp signal is greater than the threshold value; and

storing the data output signal associated with each data pulse in a shift register.

2. The data communication method of claim 1, wherein the pulse separation comprises the time duration between the trailing edge of a first data pulse and the leading edge of a second data pulse following the first data pulse, and wherein the first pulse separation is shorter than the second pulse separation.

3. The data communication method of claim 1, wherein the threshold value comprises the logic threshold of the input terminal of the shift register.

4. The data communication method of claim 1, wherein the threshold value comprises a reference voltage value and wherein the generating a data output signal associated with each data pulse having a first logical state and the generating a data output signal associated with each data pulse having a second logical state comprise:

comparing the voltage ramp signal to the reference voltage value;

generating a data output signal associated with each data pulse having the first logical state when the voltage value of the voltage ramp signal is less than the reference voltage value; and

generating a data output signal associated with each data pulse having the second logical state when the voltage value of the voltage ramp signal is greater than the reference voltage value.

5. The data communication method of claim 1, further comprising:

at the last data pulse, generating a latching pulse appended to the last data pulse, the latching pulse having a

voltage magnitude beyond a normal voltage range of the data pulses;

receiving the latching pulses at the data terminal; and

generating a latch signal in response to the latching pulse, the latch signal causing the data output signals associated with the data pulses to be stored in a memory circuit.

6. The data communication method of claim 5, wherein generating a latching pulse appended to the last data pulse comprises generating the latching pulse having a voltage magnitude greater than the Vdd voltage of the data pulses.

7. The data communication method of claim 5, wherein generating a latching pulse appended to the last data pulse comprises generating the latching pulse having a voltage magnitude less than the Vss voltage of the data pulses.

8. The data communication method of claim 1, further comprising:

at the last data pulse, generating a latching pulse appended to the last data pulse, the latching pulse having a voltage magnitude beyond a normal voltage range of the data pulses;

receiving the latching pulses at the data terminal;

when a first portion of the data output signals associated with the data pulses corresponds to a first program code, generating a latch signal in response to the latching pulse, the latch signal causing a second portion of the data output signals associated with the data pulses to be stored in a memory circuit.

9. The data communication method of claim 8 wherein the digital data to be transmitted at the data terminal comprises N bits of digital data encoded in N data pulses, the first portion of the data output signals comprising P bits of the digital data and the second portion of the data output signals comprising at least N-P bits of the digital data.

10. The data communication method of claim 1, further comprising:

at the last data pulse, generating a latching pulse appended to the last data pulse, the latching pulse having a voltage magnitude beyond a normal voltage range of the data pulses;

receiving the latching pulses at the data terminal;

when the data output signals associated with the data pulses correspond to a first program code, generating a latch signal in response to the latching pulses; and

erasing data stored in a memory circuit in response to the latch signal.

11. The data communication method of claim 1, wherein:

generating a voltage ramp signal comprises charging a capacitor to the first voltage;

resetting the voltage ramp signal a given delay after the leading edge of each data pulse comprises shorting the capacitor to the second voltage; and

detecting the voltage value of the voltage ramp signal at the leading edge of each data pulse comprises measuring the voltage value of the capacitor at the leading edge of each data pulse.

12. The data communication method of claim 1, wherein:

generating a voltage ramp signal comprises discharging a capacitor to the first voltage;

resetting the voltage ramp signal a given delay after the leading edge of each data pulse comprises shorting the capacitor to the second voltage; and

detecting the voltage value of the voltage ramp signal at the leading edge of each data pulse comprises measuring the voltage value of the capacitor at the leading edge of each data pulse.

13. The data communication method of claim 1, wherein regenerating the voltage ramp signal a first time period after the resetting of the voltage ramp signal comprises:

regenerating the voltage ramp signal at the trailing edge of each data pulse or a second delay after the trailing edge of each data pulse.

14. The data communication method of claim 1, wherein regenerating the voltage ramp signal a first time period after the resetting of the voltage ramp signal comprises:

regenerating the voltage ramp signal after the resetting of the voltage ramp signal, the first time period comprising a zero time period.

15. The data communication method of claim 13, wherein the leading edge of the data pulses comprises the rising edge of the data pulses and the trailing edge of the data pulses comprises the falling edge of the data pulses.

16. A data communication method for transmitting and receiving serial digital data over a single communication line:

encoding data to be transmitted as data pulses, the data pulses having a first pulse separation to represent a first logical data value and a second pulse separation to represent a second logical data value;

transmitting the data pulses on a single communication wire;

receiving the data pulses at a data terminal;

generating a voltage ramp signal having a voltage magnitude between a first voltage and a second voltage;

resetting the voltage ramp signal to the first voltage a first delay after the leading edge of each data pulse;

regenerating the voltage ramp signal towards the second voltage a first time period after the resetting of the voltage ramp signal;

detecting the voltage value of the voltage ramp signal at the leading edge of each data pulse;

generating a data output signal associated with each data pulse having a first logical state when the voltage value of the voltage ramp signal is less than a threshold value;

generating a data output signal associated with each data pulse having a second logical state when the voltage value of the voltage ramp signal is greater than the threshold value; and

storing the data output signal associated with each data pulse in a shift register.

17. An integrated circuit, comprising:

a data terminal, the data terminal to be coupled to a single data wire for receiving digital data transmitted on the single data wire; and

a serial data interface circuit comprising:

a first terminal coupled to the data terminal for receiving the digital data, the digital data being encoded as data pulses having a first pulse separation to represent a first logical data value and a second pulse separation to represent a second logical data value;

a delay circuit comprising an input terminal coupled to the data terminal for receiving the data pulses and an output terminal providing an output signal, the delay circuit introducing a first delay to at least the leading edge of each data pulse and providing delayed data pulses as the output signal at the output terminal;

a ramp signal circuit comprising a control input terminal coupled to receive the output signal of the delay circuit and an output terminal providing a voltage ramp signal having a voltage magnitude between a first voltage and a second voltage, the voltage ramp signal being reset to the first voltage at the leading edge of each delayed data pulse and being regenerated towards the second voltage at a first time period after the leading edge of each delayed data pulse; and

an N-bit shift register having a clock input terminal coupled to the first terminal receiving the data pulses, a data input terminal coupled to the output terminal of the ramp signal circuit for receiving the voltage ramp signal and an N-bit data output terminal providing the N-bit digital data stored therein in parallel data bits,

wherein for each data pulse, the shift register stores a data signal indicative of the magnitude of the voltage ramp signal at the leading edge of each data pulse, the data signal having a first logical state when the voltage value of the voltage ramp signal is less than a threshold value and the data signal having a second logical state when the voltage value of the voltage ramp signal is greater than the threshold value.

18. The integrated circuit of claim 17, wherein the pulse separation comprises the time duration between the trailing edge of a first data pulse and the leading edge of a second data pulse following the first data pulse, and wherein the first pulse separation is shorter than the second pulse separation.

19. The integrated circuit of claim 17, wherein the voltage ramp signal is regenerated at the trailing edge of each data pulse.

20. The integrated circuit of claim 17, wherein the delay circuit introduces the first delay to the leading edge and the trailing edge of each data pulse and the voltage ramp signal is regenerated at the trailing edge of each delayed data pulse.

21. The integrated circuit of claim 17, wherein the first time period for regenerating the voltage ramp signal comprises zero time period.

22. The integrated circuit of claim 17, wherein the leading edge of the data pulses comprises the rising edge of the data

pulses and the trailing edge of the data pulses comprises the falling edge of the data pulses.

23. The integrated circuit of claim 17, wherein the threshold value comprises the logic threshold of the input terminal of the shift register.

24. The integrated circuit of claim 17, wherein the threshold value comprises a reference voltage value and the integrated circuit further comprises a comparator circuit having a first input terminal coupled to the output terminal of the ramp signal circuit and a second input terminal coupled to receive the reference voltage value and an output terminal coupled to the data input terminal of the shift register.

25. The integrated circuit of claim 17, wherein the ramp signal circuit comprises:

a capacitor having a first plate coupled to a first node and a second plate coupled to the first voltage;

a current source coupled to the first plate of the capacitor for providing a source of current to charge the capacitor; and

a switch circuit coupled between the first node and the first voltage, the switch circuit being controlled by the leading edge of the delayed data pulses,

wherein at the leading edge of the delayed data pulses, the switch circuit is closed to short the first plate of the capacitor to the first voltage and after the first time period after the leading edge of the delayed data pulses, the switch circuit is open and the capacitor is charged by the current from the current source towards the second voltage.

26. The integrated circuit of claim 25, wherein the first voltage comprises a Vss voltage and the capacitor is being charged up by the current source to the second voltage being the Vdd voltage.

27. The integrated circuit of claim 25, wherein the first voltage comprises a Vdd voltage and the capacitor is being discharged by the current source to the second voltage being the Vss voltage.

28. The integrated circuit of claim 17, further comprising:

a latching circuit having a first input terminal coupled to the first terminal for receiving the data pulses, a second input terminal coupled to receive a first supply voltage of the integrated circuit and an output terminal providing a latch signal,

wherein the data pulses received at the data terminal comprise a latching pulse appended to the last one of the data pulses, the latching pulse having a voltage magnitude exceeding the first supply voltage; and

wherein the latching circuit asserts the latch signal when the latching circuit detects a data pulse having a voltage magnitude exceeding the first supply voltage, the latch signal causing the N-bit data signals stored in the shift register to be latched in a memory circuit of the integrated circuit.

29. The integrated circuit of claim 28, wherein the first supply voltage comprises a Vdd voltage and the latching pulse has a voltage magnitude greater than the first supply voltage.

30. The integrated circuit of claim 28, wherein the first supply voltage comprises a Vss voltage and the latching pulse has a voltage magnitude less than the first supply voltage.

31. The integrated circuit of claim 28, wherein the latching circuit comprises a supply exceed detector, the supply exceed detector comprising:

a first set of M serially connected diodes coupled to receive the first supply voltage and providing a first output voltage having a voltage magnitude M diode voltage drop less than the first supply voltage;

a second set of P serially connected diodes, P being greater than M, coupled to receive the data pulses and providing a second output voltage having a voltage magnitude P diode voltage drop less than the voltage magnitude of the data pulses; and

a comparator coupled to compare the first output voltage and the second output voltage, the comparator asserting the latch signal when the second output voltage is greater than the first output voltage.

32. The integrated circuit of claim 28, wherein the latching circuit comprises a supply exceed detector, the supply exceed detector comprising:

a PMOS transistor having a control terminal coupled to the first supply voltage, a first current handling terminal coupled to a current source and a second current handling terminal coupled to receive the data pulses; and

an inverter having an input terminal coupled to the first current handling terminal of the PMOS transistor and an output terminal providing the latch signal,

wherein the inverter asserting the latch signal when the voltage magnitude of the data pulses is a transistor threshold voltage greater than the first supply voltage.

33. The integrated circuit of claim 17, further comprising:

a latching circuit having a first input terminal coupled to the first terminal for receiving the data pulses, a second input terminal coupled to receive a first supply voltage of the integrated circuit, a third input terminal coupled to the output terminal of the shift register and an output terminal providing a latch signal,

wherein the data pulses received at the data terminal comprise a latching pulse appended to the last one of the data pulses, the latching pulse having a voltage magnitude exceeding the first supply voltage; and

wherein the latching circuit asserts the latch signal when the latching circuit detects a data pulse having a voltage magnitude exceeding the first supply voltage and when a first portion of the N-bit data signal stored in the shift register corresponds to a first program code, the latch signal causing a second portion of the N-bit data signal stored in the shift register to be latched in a memory circuit of the integrated circuit.

34. The integrated circuit of 33, wherein the first portion of the data output signals comprises P bits of the N-bit digital data and the second portion of the data output signals comprising at least N-P bits of the N-bit digital data.

35. The integrated circuit of 33, wherein the first program code is stored in the latching circuit.

36. The integrated circuit of 33, wherein the first program code is stored in the memory circuit of the integrated circuit and is provided to the latching circuit by the memory circuit.

37. The integrated circuit of claim 17, further comprising:

a latching circuit having a first input terminal coupled to the first terminal for receiving the data pulses, a second input terminal coupled to receive a first supply voltage of the integrated circuit and an output terminal providing a latch signal,

wherein the data pulses received at the data terminal comprise a latching pulse appended to the last one of the data pulses, the latching pulse having a voltage magnitude exceeding the first supply voltage; and

wherein the latching circuit asserts the latch signal when the latching circuit detects a data pulse having a voltage magnitude exceeding the first supply voltage and when a portion of the N-bit data signal stored in the shift register corresponds to a first program code, the latch signal causing data stored in a memory circuit of the integrated circuit to be erased.

38. The integrated circuit of claim 17, wherein the data terminal is a multi-function data terminal and the integrated circuit further comprises:

an application-specific circuit coupled to the data terminal, the application-specific circuit receiving digital data from or transmitting digital data onto the data terminal.

39. The integrated circuit of claim 38, further comprising:

a disable circuit coupled between the data terminal and the first terminal of the serial data interface circuit, the disable circuit being controlled by a mode select signal, wherein the disable circuit is disengaged to connect the first terminal of the serial data interface circuit to the data terminal when the mode select signal has a first state for activating the serial data interface circuit.

40. The integrated circuit of claim 39, wherein the disable circuit comprises a multiplexer having an input terminal coupled to the data terminal, a first output terminal coupled to the first terminal of the serial data interface circuit, a second output terminal coupled to the application-specific circuit, and a select input terminal coupled to receive the mode select signal, wherein the multiplexer connects the input terminal to the first output terminal when the mode select signal has a first state for activating the serial data interface circuit and the multiplexer connects the input terminal to the second output terminal when the mode select signal has a second state for deactivating the serial data interface circuit.

41. The integrated circuit of claim 17, wherein the N-bit shift register comprises a series of N D-flip-flops, the clock terminals of each D-flip-flop being coupled to the first terminal, the data input terminal of each D-flip-flop being coupled to the data output terminal of the prior D-flip-flop, the data input terminal of the first one of the D-flip-flop being coupled to the output terminal of the ramp signal circuit.